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REMARKS

Claims 1, 2, 4, 18, 20 to 27, 33 to 40 and 43 were pending in the application at the time of final examination. Claim 27 stands rejected as anticipated. Claims 1, 2, 4, 18, 20, 21, 22 and 33 to 40 stand rejected as obvious. Claims 23 to 26 stand objected to for being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claim 43 stands allowed.

Applicants acknowledge a telephone conversation with the Examiner noting that the Action issued on 11/26/2008 failed to address Applicants' remarks that Kanakogi was not a proper reference. The new action issued on 02/06/2009 acknowledged Applicants' remarks and cited to the Examiner's Answer on May 5, 2006. However, the final action failed to address the substance of Applicants' prior remarks which asserted that the Examiner's Answer was incorrect. Applicants expressly pointed out the basis for that assertion. (See Pg. 11, last two paragraphs; Pg. 12, last paragraph; Pg. 14, fourth paragraph of paper dated July 3, 2008)

Thus, the final action is still incomplete because Applicants have no basis for knowing why the prior remarks were not persuasive. In addition, the Board of Appeals directed that the Examiner vacate the Examiner's Answer relied upon in the rejection, i.e.,

> To correct this problem, **the examiner will need to vacate the Examiner's Answer mailed May 5, 2006. Once the Examiner's Answer mailed May 5, 2006 is vacated**, the examiner has the following options: (Emphasis Added.)
>
> . . . .
>
> Accordingly, it is

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ORDERED that the application is returned to the examiner to:

1) vacate the Examiner's Answer mailed May 5, 2006:

Order Returning Undocketed Appeal to Examiner, at pg. 5, Mailed December 5, 2006.

Thus, it is unclear how the Office can rely upon something that has been vacated. In view of these problems, the application is not ready for appeal and so the finality of the rejection should be withdrawn. Applicants should not be forced to file yet another appeal based upon an incomplete record.

Also, in the prior response, Applicants asserted that the interpretation of Kanakogi was incorrect with respect to Claims 4, 37, 20 and 21 and that a non-existent Figure has been cited in the rejection of Claim 22. Nevertheless, the prior rejections were simply repeated in this action and Applicants' remarks were not addressed. Also, the rejection failed to explain how the cited sections could be relied upon in view of the fact that Kanakogi had been modified by the Office. Thus, the final rejection is incomplete for multiple reasons and the finality should be withdrawn.

Applicants respectfully traverse the Office's characterization of Kanakogi as a proper reference and submit that the reliance on the vacated Examiner's Answer is misplaced. As previously pointed out, the Examiner was able to determine the scope of Applicants' invention and to determine what Applicants were in possession of in the Examiner's Answer. The remarks in Reply Brief (37 C.F.R. § 41.41) dated July 5, 2006 are incorporated herein by reference, because the Office has failed to explain why these remarks are not persuasive.

In addition, Applicants note that the claimed invention subject matter need not be described literally, i.e., using the same terms, for the disclosure to satisfy the description requirement. MPEP § 2106, B. 1., 8th Ed., Rev 6., pg. 2100-14

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(Sept. 2007). "[T]he 'essential goal' of the description of the invention requirement is to clearly convey the information that an applicant has invented the subject matter which is claimed." MPEP § 2163 I., 8th Ed., Rev 6., pg. 2100-172 (Sept. 2007). "An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention." MPEP § 2163 I., 8th Ed., Rev 6., pg. 2100-173 (Sept. 2007).

Applicants have demonstrated on the record that the parent application described the invention using words, and formulas. See Appellant's Brief (Revised) (37 C.F.R. § 41.37), pgs. 7 to 20, dated February 7, 2006, which are incorporated herein by reference. In addition, the Office demonstrated unequivocally that description requirement was met by characterizing the invention in the Examiner's answer based on that description. The Examiner's Answer demonstrates that the Office was able to determine what Applicants were in possession of based on only the parent application.

The fact that the claims have breadth, as demonstrated in the Examiner's Answer, does not mean that the claims are not adequately described. The Office was able to ascertain what Applicants were in possession of as well as the breadth of that possession. Thus, the Office demonstrated that one of skill not only could determine what Applicants were in possession of, but also could determine the metes and bounds of that possession. Accordingly, rather than support the continued reliance upon Kanakogi as a reference, the Examiner's Answer demonstrates that the parent application complied with all 112 requirements and so Kanakogi is not a proper reference and should be withdrawn.

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Claim 27 stands rejected under § 102(e) as being anticipated by U.S. Patent No. 6,609,143, hereinafter referred to as Kanakogi.

Applicants respectfully traverse the anticipation rejection of Claim 27. As discussed more completely below, a prima facie anticipation rejection has not been made and even if a prima facie anticipation rejection were made, Kanakogi is not a proper reference. Thus, the rejection of Claim 27 is not well founded for multiple reasons.

Applicants respectfully note that it is not enough that Kanakogi show similar features, but rather the MPEP requires:

> **TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM**
>
> . . . ."The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

MPEP § 2131, 8 Ed., Rev. 6, p. 2100-67 (Sept. 2007). The MPEP demonstrates that it is not sufficient that Kanakogi generally shows the invention. Rather, Kanakogi must show the invention in as complete detail as contained in the Claims. However, even this is not enough, Kanakogi must also show the elements arranged as required by the claim. The rejection, as demonstrated below, fails to meet the criteria put forth in the MPEP and so a prima facie anticipation rejection has not been made.

Applicants note that Claim 27 recites:

> an instruction sequence, the instruction sequence including an instance of a parallel multiply add instruction;

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the instance of the parallel multiply add instruction having an at least four operand instruction format

The rejection has cited no teaching or suggestion of such an instruction in Kanakogi. Claim 27 positively recites a parallel multiply-add instruction having a least four operands.

Kanakogi describes that the configuration of Fig. 12 receives two input data words X and Y (Kanakogi, Col. 1, lines 30 to 32) and outputs a number Z. Accordingly, Kanakogi fails to teach or suggest anything about an instruction having at least four operands, by explicitly describing two input operands X and Y and one result Z. Kanakogi discloses a configuration in which an addend is clearly not sourced from an input operand specified by a parallel multiply-add instruction as recited in Claim 27. Rather, register 105 (see Kanakogi, FIG. 12 and accompanying description in Cols. 1 and 2) appears to be an accumulate register internal to the multiply-accumulate functional unit depicted. No instruction-specifiable source register of an operand is disclosed.

Moreover, the rejection has failed to cite to any teaching of storing the first sum in accordance with a fourth operand's first component as recited in Claim 27. The rejection has not even identified with any specificity what is considered the fourth operand and instead relies upon Applicants' claim language. Therefore, for Claim 27, Kanakogi is non-anticipatory and there is no teaching or suggestion in the art of record for a modification that would introduce into the critical path, significant register access latencies unnecessary (and arguably undesirable) for the multiply-accumulate functional unit disclosed in Kanakogi.

Accordingly, Kanakogi fails to show the invention in as complete detail as contained in these claims. According to the MPEP, as quoted above, this alone is sufficient to overcome the anticipation rejection.

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If necessary, to preserve the remarks for appeal, Applicants have demonstrated that Kanakogi is not a proper reference. In addition to the above remarks, in the paper dated February 7, 2006 and entered on February 23, 2006 by the Office, at pgs. 15 to 17, Applicants demonstrated that the parent application fully described and supported Claim 27. In the paper filed on July 5, 2006 and entered by the USPTO on July 5, 2006, Applicants rebutted the Office's position and demonstrated that it was not well founded at pages 4 and 5, which are incorporated herein by reference.

Accordingly, Kanakogi is not a proper reference and so not only has a prima facie anticipation rejection not been made, but also the reference is not proper. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claim 27.

Claims 1, 2, 4, 18, 20, 21, and 33 to 40 stand rejected under § 103(a) as being unpatentable over U.S. Patent No. 6,609,143, hereinafter referred to as Kanakogi, in view of U.S. Patent No. 6,725,355, hereinafter referred to as Imamura.

Applicants respectfully traverse the obviousness rejection of each of Claims 1, 18, and 33. With respect to an obviousness rejection, all words in a claim must be considered in judging the patentability of that claim against the prior art. MPEP § 2143.03, 8th Ed., Rev. 6, p. 2100-142 (Sept. 2007). This is a fundamental aspect in the requirement that **"THE CLAIMED INVENTION AS A WHOLE MUST BE CONSIDERED."** MPEP § 2141.02 I., 8th Ed., Rev. 6, p. 2100-123 (Sept. 2007).

Using Claim 1, as an example, the parallel multiply-add instruction is indicated by an opcode and has at least three operands (Claim 1, lines 4 to 6). Operand one has a first value; operand two has a second value; and operand three has a third value. (Claim 1, lines 7 to 10.)

The three operands are different from the result, because the claim recites "a result location," (Claim 1, lines 24 and

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26), which is different from the operands. Further, the plain meaning of the operations in the claims is that the operands are source operands and not intermediate values, because the operands are included with the instruction.

This interpretation of Claim 1 follows directly from the plain meaning of the claim and relies upon only the claim language itself. The MPEP requires that "words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification." MPEP § 2111.01, I., 8th Ed. Rev. 6, p 2100-38 (September 2007).

In an obviousness rejection, the MPEP also requires that the references be considered as a whole. When Kanakogi and Imamaura are considered as a whole, the two references are at most cumulative and so fail to suggest Applicants' invention as recited in these claims.

First, Imamaura defines a two operand instruction as having two operands designating a source register and a destination register. Imamura, Col. 11, lines 22 to 25. Similarly, a three operand instruction is described as requiring two read ports and a write port. Imamura, Col. 2, lines 11 to 14. Thus, a three operand instruction according to Imamura has two source operands that are read via the read ports and a result operand that is written via the write port.

Thus, in considering Imamaura as a whole, the section cited in the rejection must be interpreted in view of Imamaura's definition of a three operand instruction and a two operand instruction. The cited section stated:

> Also, according to the microprocessor 81, it is possible to access three different three bits of data in the internal memory 87 in the same clock cycle using a two-operand processing instruction and to real processing substantially similar to three-operand processing

The three-operand processing referred to here, in view of the earlier definition, is two sources and one result as

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opposed to the two-operand processing, which is one source and one result. However, as noted above, Kanakogi taught in Fig. 12, two sources X and Y and one result Z. Thus, Imamura and Kanakogi are at best cumulative, when the references are considered as a whole. The proposed modification based on the teachings in Imamaura results in nothing other than what is already taught by Kanakogi.

Neither reference, nor the combination, suggests any process utilizing three source operands and a result. Moreover, with respect to processor architecture, both Imamaura and Kanakogi show that specific hardware configurations are required to support particular sets of instructions.

Accordingly, it requires more than a generalized statement to extract a statement concerning execution of instructions with one processor configuration to utilize the teaching in a different processor configuration. In particular, the rejection has failed to explain how the accumulate process of Kanakogi would work when more than two source operands are used. In addition, Kanakogi taught that the configuration of Fig. 12 was undesirable and taught a different architecture was required to achieve the desired results.

The rejection ignores this teaching and simply asserts processing that was possible using the architecture of Imamura could be extracted and used in a completely different architecture that was described as being unsatisfactory to Kanakogi. The addition of another source operand to Kanakogi requires additional wiring and moving of data to perform the accumulate function of Kanakogi. Since the configuration described in Fig. 12 was unacceptable to Kanakogi, Kanakogi establishes that the proposed further modification would not be acceptable and would not function as properly according to Kanakogi. Thus, according to the MPEP, the combination of references is not appropriate.

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Finally, the rationale for the combination relies upon "to arrive at the conditional pick instruction." Claim 1 does not recite such an instruction and so the rationale for the combination has nothing to do with the recitation in Claim 1 and so is inappropriate. Applicants respectfully request reconsideration and withdrawal of the obviousness rejection of each of Claim 1, 18 and 33.

Applicants respectfully traverse the obviousness rejection of each of Claims 2, 4, and 35 to 38. Claims 2 and 4 depend from Claim 1 and so distinguish over the combination of references for at least the same reasons as Claim 1. Claims 35 to 38 depend from Claim 33 and so distinguish over the combination of references for at least the same reasons as Claim 33.

The rejection of Claims 4 and 37 cites only to Kanakogi and reduces the express claim limitations to a gist, "two signals would have to be completed before the results were stored." Claim 4, as an example, recites "executed with a throughput of one instruction every 2 cycles." The fact that two cycles would have to be completed suggests or discloses nothing about throughput. Therefore, a prima facie obviousness rejection has not been made.

Claims 4 and 37 positively recite attributes of pipeline performance and despite the rejection having been traversed, the rejection is simply repeated without any consideration of Applicants' prior remarks. This is a further indication that the final rejection is incomplete.

Kanakogi's configuration cannot support the recited cycling and the modifications would further complicate the configuration. Since register 105 in Fig. 12 of Kanakogi constitutes both a source and a sink for add operations, this register cannot simultaneously act as a current addend source (and target) as well as the target of an additional undisclosed (but hypothetical) operation to preload an addend for use in a

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subsequent pipelined operation. A throughput of one parallel multiply-add instruction every 2 cycles is simply not compatible with Kanakogi's disclosed configuration. Applicants respectfully request reconsideration and withdrawal of the obviousness rejection of each of Claims 4 and 37.

Applicants respectfully traverse the obviousness rejection of each of Claims 20 and 21, which depend from Claim 18. Again, the prior rejection has simply been repeated including comments that are no longer correct with respect to the dependency of these claims. The rejection fails to address the modified form of Kanakogi and instead relies only on teachings of Kanakogi that are not associated with Fig. 12, but instead are associated with Fig. 2. Applicants note that no rationale has been provided for extracting a feature of Fig. 2 and including that feature in Fig. 12 which was relied upon with respect to Claim 1.

In addition, the Office relies on disclosure in Kanakogi which has nothing to do with either the saturated arithmetic recited in these claims or the functional unit illustrated in FIG. 12 of Kanakogi. Rather, the rejection relied upon disclosure that concerns a data extended shifter 55 employed in the configuration of FIG. 2 of Kanakogi, which does not correspond to Applicants' claims.

The disclosed data extender/shifter appears to be unrelated to saturated arithmetic and no teaching or suggestion exists (in Kanakogi or any other art of record) to include data extender/shifter 55 to support saturated arithmetic in the dissimilar multiply accumulate functional unit disclosed by Kanakogi in FIG. 12. Thus, Claims 20 and 21 distinguish over the combination or reerences for reasons in addition to those given above for Claim 18. Applicants respectfully request reconsideration and withdrawal of the obviousness rejection of Claims 20 and 21.

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Claims 39 and 40 depend from Claim 18 and so distinguish over the combination of references for at least the same reasons as Claim 18. Applicants respectfully request reconsideration and withdrawal of the obviousness rejection of each of Claims 39 and 40.

Claim 22 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanakogi and Imamaura in view of U.S. Patent No. 6,490,607 to Oberman and further in view of Hennessy.

As discussed above with reference to the claims rejected under § 103, Applicants are entitled to the priority date of US Application 09/204,480, now US Patent 6,718,457. That priority date, December 3, 1998 antedates Kanakogi's effective filing date of July 20, 2000. A proper claim of priority has been made and Applicants have provided detailed support in the priority application sufficient under 35 U.S.C. § 112 for Claim 22. Because this claim has § 112 support in the '457 patent, Kanakogi is not prior, and so Kanakogi does not constitute prior art under § 103(a). Thus, a prima facie obviousness rejection has not been made.

Moreover, even if the combination of three references were correct, the combination fails to disclose or suggest processor support for a conditional pick instruction as claimed. For disclosure of the conditional pick instruction, the Office refers to a Figure 14, which does not exist in Oberman, a section of Oberman that discloses branch prediction, and a branch on not equal to zero instruction from Hennessy. The Office assumes that a branch on not equal to zero (bne) instruction must co-exist with branch prediction. A bne instruction does not disclose or suggest a conditional pick instruction. The claimed conditional pick instruction compares a first value to zero and then copies either a second or a third value to a destination depending on the comparison. A bne instruction compares a first value to zero, and either branches or continues. It is clear that these two instructions

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perform different operations. Accordingly, the combination does not add the disclosure of processor support for a conditional pick instruction missing from Kanakogi and claim 22 is allowable for at least this reason.

Claims 1, 2, 4, 18, 20 to 27, 33, and 35 to 43 remain in the application. Claims 5 to 17 stand withdrawn. Claims 3, 5 to 17, 19, 28 to 32, and 34 were canceled previously. For the foregoing reasons, Applicant(s) respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office, Fax No.571-273-8300, on April 3, 2009.

Mona Marshall — April 3, 2009
Mona Marshall — Date of Signature

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